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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/773,872	02/02/2001	Richard Bullock	ESM00-001	7976

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EXAMINER	
BOOTH, RICHARD A	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/773,872	BULLOCK ET AL.	
	Examiner	Art Unit	
	Richard A. Booth	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5-27-03 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyasaka, U.S. Patent 6,124,154 in view of Kuo et al., U.S. Patent 5,981,347.

Miyasaka shows the invention as claimed including providing said insulating substrate; forming an active semiconductor layer on said insulating substrate; thermally depositing a silicon oxide gate dielectric layer on said active semiconductor layer, using TEOS (see col. 17-lines 17-33); and performing an anneal procedure to densify said silicon oxide gate dielectric layer (see Fig. 1 and col 15-line 15 to col. 18-line 2). Miyasaka, U.S. Patent 6,124,154 is applied as above but lacks anticipation of specific

processing conditions with respect to the polysilicon layer and the thermal oxidation and densification processes, and performing a first anneal procedure subsequent to growing said first dielectric layer.

Kuo et al. discloses performing a high temperature anneal after gate oxide formation so as to activate the source/drain regions (see abstract). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Miyasaka so as to perform an anneal process subsequent to the gate oxide formation in order to activate the source/drain dopants so as to have a functioning device. Furthermore, as previously stated, the examiner takes official notice that these parameters are typical well known processing conditions suitable, for example, to form thermal dielectrics or for oxide densification. Furthermore, since the official notice has been challenged with respect to the thickness of the composite gate oxide, Yamazaki, U.S. Patent 6,306,213 B1 shows a gate dielectric layer deposited to a thickness between 500-2000 angstroms (see col. 8-lines 11-17). In view of this disclosure, it would have been obvious to one of ordinary skill in the art that a prima facie case of obviousness exists with respect to forming a gate dielectric with a thickness ranging from 550-850 angstroms because in the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990).

Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al., U.S. Patent 6,037,199 in view of Doklan et al., U.S. Patent 4,851,370 or Kuo et al., U.S. Patent 5,981,347.

Huang et al. shows the invention substantially as claimed including an insulating substrate 1; an active semiconductor layer of polysilicon 5 with a thickness of 300-1000 angstroms (see col. 3-lines 6-28); forming a gate dielectric layer 9 on said active semiconductor layer; depositing a second polysilicon layer 10 on said gate dielectric; patterning said gate electrode and gate dielectric layer (see Figs. 6-7); and forming a source/drain region 11 in a portion of said polysilicon layer not covered by said polysilicon gate structure (see Figures 1-7 and column 2-line 51 to column 4-line 33).

Huang et al. lacks anticipation of forming a composite gate dielectric layer comprising a first thermally grown oxide layer, followed by an annealing process, a second thermally deposited oxide layer using a TEOS source, and a second subsequent anneal.

Doklan et al. discloses forming a composite gate dielectric structure on a silicon substrate 1 using a first thermally grown oxide layer 3 of fifty angstroms followed by a subsequent thermal deposition of an oxide layer 5 using a TEOS source (see col. 3-line 63 to col. 4-line 7). Note that a first anneal is performed after the thermally grown layer 3 is formed in an argon atmosphere and a second subsequent anneal was used after formation of the TEOS based layer to densify the oxide (see col. 8-lines 8-14). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the primary reference of Huang et al. so as to

incorporate the composite gate dielectric of Doklan et al. because this results in a gate dielectric with low defect density (see abstract). Alternatively, Kuo et al. discloses performing a high temperature anneal after gate oxide formation so as to activate the source/drain regions (see abstract). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Huang et al. so as to perform an anneal process subsequent to the gate oxide formation in order to activate the source/drain dopants so as to have a functioning device.

With respect to processing parameters such as the thicknesses of layers and conditions of oxidations and anneals, the examiner takes official notice that these parameters in the claims are typical well known processing conditions suitable, for example, to form thermal dielectrics or for oxide densification. Furthermore, since the official notice has been challenged with respect to the thickness of the composite gate oxide, in response, Yamazaki, U.S. Patent 6,306,213 B1 shows a gate dielectric layer deposited to a thickness between 500-2000 angstroms (see col. 8-lines 11-17) on a layer that is at least partially polycrystalline (see col. 7-lines 29-56). In view of this disclosure, it would have been obvious to one of ordinary skill in the art that a prima facie case of obviousness exists with respect to forming a gate dielectric with a thickness ranging from 550-850 angstroms because in the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990).

Response to Arguments

Applicant's arguments filed 5-27-03 have been fully considered but they are not persuasive. Applicant argues that none of the references recognize the use of a polysilicon layer. However, both Huang et al. (see col. 3-lines 5-27) and Miyasaka (see col. 17-lines 42-45) disclose the use of a polysilicon layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard A. Booth whose telephone number is 308-3446. The examiner can normally be reached on Monday-Thursday from 7:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are 308-7724 for regular communications and 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 308-1782.

Richard A. Booth
Primary Examiner
Art Unit 2812